1. A chip mounting system comprising:

a substrate for mounting at least one chip, said substrate having at least one through-hole; and

a multi-layer structure covering both sides of said substrate and passing through said at least one through-hole, said multi-layer structure comprising at least one conductive plane and a signal wiring layer, said at least one conductive plane and said signal wiring layer having an insulating layer interposed between them.

2. The chip mounting system of claim 1, wherein said conductive plane comprises a first ground plane.

3. The chip mounting system of claim 2, wherein said first ground plane is at least 3 μm thick.

4. The chip mounting system of claim 2, wherein the thickness of said first ground plane is less than or equal to 5 μm.

5. The chip mounting system of claim 1, wherein said conductive plane comprises a power supply distribution plane.

6. The chip mounting system of claim 1, wherein said conductive plane comprises a copper plane.

7. The chip mounting system of claim 1, wherein said conductive plane comprises an aluminum plane.

8. The chip mounting system of claim 1, wherein said multi-layer structure further comprises a first insulating layer provided on the side said multi-layer structure directly adjacent to said substrate.

9. The chip mounting system of claim 8, wherein said first insulating layer comprises a silicon dioxide layer.

10. The chip mounting system of claim 9, wherein the thickness of said silicon dioxide layer is 0.1 to 0.5μm.

11. The chip mounting system of claim 8, wherein said conductive plane is deposited over said first insulating layer.

12. The chip mounting system of claim 1, wherein said insulating layer comprises a second insulating layer formed over said conductive plane.

13. The chip mounting system of claim 1, wherein said multi-layer structure further comprises a third insulating layer formed over said signal wiring layer.

14. The chip mounting system of claim 13, wherein said multi-layer structure further comprises a second conductive plane formed over said third insulating layer.

15. The chip mounting system of claim 12, wherein said second insulating layer comprises silicon dioxide.

16. The chip mounting system of claim 12, where the thickness of said second insulating is 0.5 to 4.0μm.

17. The chip mounting system of claim 1, wherein said signal wiring layer comprises at least one signal line.

18. The chip mounting system of claim 17, wherein said at least one signal line is 6 to 10 μm wide.

19. The chip mounting system of claim 13, wherein said third insulating layer comprises a silicon dioxide layer.

20. The chip mounting system of claim 14, wherein the thickness of said second conductive plane is 3 μm to 5 μm.

21. The chip mounting system of claim 17, wherein said at least one signal line is terminated at a bond pad.

22. The chip mounting system of claim 12, wherein said second insulating layer comprises a polyimide layer.

23. The chip mounting system of claim 13, wherein said third insulating layer comprises a silicon dioxide layer.

24. The chip mounting system of claim 13, wherein said third insulating layer comprises a polyimide layer.

25. The chip mounting system of claim 14, wherein said second conductive plane comprises a ground plane.

26. The chip mounting system of claim 14, wherein said second conductive plane comprises a power supply distribution plane.

27. The chip mounting system of claim 14, wherein said multi-layer structure further comprises a fourth insulating layer formed over said second conductive plane.

28. A chip mounting system comprising:

a substrate for mounting at least one chip, said substrate having at least one through-hole;

a multi-layer structure covering both sides of said substrate and passing through said through-hole, said multi-layer structure comprising a conductive plane and a signal wiring layer having traces terminating in bond pads, said conductive plane and said signal wiring layer having an insulating layer interposed between them; and

said at least one chip mounted onto said bond pads.

29. The chip mounting system of claim 28, wherein said through-hole is rectangular in shape.

30. The chip mounting system of claim 28, wherein said through-hole is circular in shape.

31. The chip mounting system of claim 28 further comprising interconnect wiring to carry a signal between said bond pads and respective traces of said signal wiring layer.

32. The chip mounting system of claim 28 further comprising interconnect wiring to carry a signal between respective traces of said signal wiring layer and active and/or passive components on the surface of said substrate.

33. The chip mounting system of claim 28, wherein said conductive plane comprises a first ground plane.

34. The chip mounting system of claim 34, wherein said first ground plane is at least 3 μm thick.

35. The chip mounting system of claim 34, wherein the thickness of said first ground plane is less than or equal to 5 μm.

36. The chip mounting system of claim 28, wherein said conductive plane comprises a power supply distribution plane.

37. The chip mounting system of claim 28, wherein said conductive plane comprises a copper plane.

38. The chip mounting system of claim 28, wherein said conductive plane comprises an aluminum plane.

39. The chip mounting system of claim 28, wherein said multi-layer structure further comprises a first insulating layer provided on the side said multi-layer structure directly adjacent to said substrate.

40. The chip mounting system of claim 39, wherein said first insulating layer comprises a silicon dioxide layer.

41. The chip mounting system of claim 40, wherein the thickness of said silicon dioxide layer is 0.1 to 0.5μm.

42. The chip mounting system of claim 39, wherein said conductive plane is deposited over said first insulating layer.

43. The chip mounting system of claim 28, wherein said insulating layer comprises a second insulating layer formed over said conductive plane.

44. The chip mounting system of claim 28, wherein said multi-layer structure further comprises a third insulating layer formed over said signal wiring layer.

45. The chip mounting system of claim 44, wherein said multi-layer structure further comprises a second conductive plane formed over said third insulating layer.

46. The chip mounting system of claim 43, wherein said second insulating layer comprises silicon dioxide.

47. The chip mounting system of claim 43, where the thickness of said second insulating is 0.5 to 4.0μm.

48. The chip mounting system of claim 28, wherein said signal wiring layer comprises at least one signal line.

49. The chip mounting system of claim 48, wherein said at least one signal line is 6 to 10 μm wide.

50. The chip mounting system of claim 44, wherein said third insulating layer comprises a silicon dioxide layer.

51. The chip mounting system of claim 45, wherein the thickness of said second conductive plane is 3 μm to 5 μm.

52. The chip mounting system of claim 48, wherein said at least one signal line is terminated at a bond pad.

53. The chip mounting system of claim 43, wherein said second insulating layer comprises a polyimide layer.

54. The chip mounting system of claim 44, wherein said third insulating layer comprises a silicon dioxide layer.

55. The chip mounting system of claim 44, wherein said third insulating layer comprises a polyimide layer.

56. The chip mounting system of claim 45, wherein said second conductive plane comprises a ground plane.

57. The chip mounting system of claim 45, wherein said second conductive lane comprises a power supply distribution plane.

58. The chip mounting system of claim 45, wherein said multi-layer structure further comprises a fourth insulating layer formed over said second conductive plane.

59. A processor system comprising:

a processor; and

memory device coupled to said processor, said processor and memory device residing on a common substrate, said substrate having a through-hole, said substrate further comprising a top side and a bottom side with multi-layer structure interposed on both sides of said substrate and passing through said through-hole, said multi-layer structure comprising:

a conductive plane; and

a signal wiring layer, said conductive plane and said signal wiring layer having an insulating layer interposed between them.

60. The processor system of claim 59, wherein said conductive plane comprises a first ground plane.

61. The processor system of claim 60, wherein said first ground plane is at least 3 μm thick.

62. The processor system of claim 60, wherein the thickness of said first ground plane is less than or equal to 5 μm.

63. The processor system of claim 59, wherein said conductive plane comprises a power supply distribution plane.

64. The processor system of claim 59, wherein said conductive plane comprises a copper plane.

65. The processor system of claim 59, wherein said conductive plane comprises an aluminum plane.

66. The processor system of claim 59, wherein said multi-layer structure further comprises a first insulating layer provided on the side said multi-layer structure directly adjacent to said substrate.

67. The processor system of claim 66, wherein said first insulating layer comprises a silicon dioxide layer.

68. The processor system of claim 67, wherein the thickness of said silicon dioxide layer is 0.1 to 0.5μm.

69. The processor system of claim 66, wherein said conductive plane is deposited over said first insulating layer.

70. The processor system of claim 59, wherein said insulating layer comprises a second insulating layer formed over said conductive plane.

71. The processor system of claim 59, wherein said multi-layer structure further comprises a third insulating layer formed over said signal wiring layer.

72. The processor system of claim 71, wherein said multi-layer structure further comprises a second conductive plane formed over said third insulating layer.

73. The processor system of claim 70, wherein said second insulating layer comprises silicon dioxide.

74. The processor system of claim 70, where the thickness of said second insulating is 0.5 to 4.0μm.

75. The processor system of claim 59, wherein said signal wiring layer comprises at least one signal line.

76. The processor system of claim 75, wherein said at least one signal line is 6 to 10 μm wide.

77. The processor system of claim 71, wherein said third insulating layer comprises a silicon dioxide layer.

78. The processor system of claim 72, wherein the thickness of said second conductive plane is 3 μm to 5 μm.

79. The processor system of claim 75, wherein said at least one signal line is terminated at a bond pad.

80. The processor system of claim 70, wherein said second insulating layer comprises a polyimide layer.

81. The processor system of claim 71, wherein said third insulating layer comprises a silicon dioxide layer.

82. The processor system of claim 71, wherein said third insulating layer comprises a polyimide layer.

83. The processor system of claim 72, wherein said second conductive plane comprises a ground plane.

84. The processor system of claim 72, wherein said second conductive plane comprises a power supply distribution plane.

85. The processor system of claim 72, wherein said multi-layer structure further comprises a fourth insulating layer formed over said second conductive plane.

86. A integrated circuit package comprising:

a substrate for mounting at least one chip, said substrate having at least one through-hole;

a multi-layer structure covering both sides of said substrate and passing through said through-hole, said multi-layer structure comprising a conductive plane and a signal wiring layer, said conductive plane and said signal wiring layer having an insulating layer interposed between them; and

a integrated circuit package to encase said substrate, said multi-layer structure and at least one circuit chip.

87. The integrated circuit package of claim 86, wherein said conductive plane comprises a first ground plane.

88. The integrated circuit package of claim 87, wherein said first ground plane is at least 3 μm thick.

89. The integrated circuit package of claim 87, wherein the thickness of said first ground plane is less than or equal to 5 μm.

90. The integrated circuit package of claim 86, wherein said conductive plane comprises a power supply distribution plane.

91. The integrated circuit package of claim 86, wherein said conductive plane comprises a copper plane.

92. The integrated circuit package of claim 86, wherein said conductive plane comprises an aluminum plane.

93. The integrated circuit package of claim 86, wherein said multi-layer structure further comprises a first insulating layer provided on the side said multi-layer structure directly adjacent to said substrate.

94. The integrated circuit package of claim 93, wherein said first insulating layer comprises a silicon dioxide layer.

95. The integrated circuit package of claim 94, wherein the thickness of said silicon dioxide layer is 0.1 to 0.5μm.

96. The integrated circuit package of claim 93, wherein said conductive plane is deposited over said first insulating layer.

97. The integrated circuit package of claim 86, wherein said insulating layer comprises a second insulating layer formed over said conductive plane.

98. The integrated circuit package of claim 86, wherein said multi-layer structure further comprises a third insulating layer formed over said signal wiring layer.

99. The integrated circuit package of claim 98, wherein said multi-layer structure further comprises a second conductive plane formed over said third insulating layer.

100. The integrated circuit package of claim 97, wherein said second insulating layer comprises silicon dioxide.

101. The integrated circuit package of claim 97, where the thickness of said second insulating is 0.5 to 4.0μm.

102. The integrated circuit package of claim 86, wherein said signal wiring layer comprises at least one signal line.

103. The integrated circuit package of claim 102, wherein said at least one signal line is 6 to 10 μm wide.

104. The integrated circuit package of claim 98, wherein said third insulating layer comprises a silicon dioxide layer.

105. The integrated circuit package of claim 99, wherein the thickness of said second conductive plane is 3 μm to 5 μm.

106. The integrated circuit package of claim 102, wherein said at least one signal line is terminated at a bond pad.

107. The integrated circuit package of claim 97, wherein said second insulating layer comprises a polyimide layer.

108. The integrated circuit package of claim 98, wherein said third insulating layer comprises a silicon dioxide layer.

109. The integrated circuit package of claim 98, wherein said third insulating layer comprises a polyimide layer.

110. The integrated circuit package of claim 99, wherein said second conductive plane comprises a ground plane.

111. The integrated circuit package of claim 99, wherein said second conductive plane comprises a power supply distribution plane.

112. The integrated circuit package of claim 99, wherein said multi-layer structure further comprises a fourth insulating layer formed over said second conductive plane.

113. A method of forming a chip carrier, said method comprising:

forming a conductive plane on both sides of a substrate and in at least one through-hole of said substrate;

forming at least one insulating layer over said conductive plane and in at least one through-hole of said substrate; and

forming a signal wiring layer over said at least one insulating layer and in at least one through-hole of said substrate.

114. The method of claim 113, wherein said forming of said at least one insulating layer comprises forming a silicon dioxide layer.

115. The method of claim 113, wherein said forming of said conductive plane is by simple evaporation.

116. The method of claim 113, wherein said forming of said conductive plane is by sputtering.

117. The method of claim 113, wherein said forming of said conductive plane is by electroplating.

118. The method of claim 113, wherein said forming of said at least one insulating layer is by chemical vapor deposition.

119. The method of claim 113, wherein said forming of said at least one insulating layer is by spin coating.

120. The method of claim 113, wherein said forming of said signal wiring layer comprises forming at least one signal line.

121. The method of claim 120, wherein said forming of said at least one signal line is by optical lithography.

122. The method of claim 120, wherein said forming of said at least one signal line is by optical lithography followed by additive metallization.

123. The method of claim 122, wherein said additive metallization is performed by liftoff by evaporation.

124. The method of claim 123, wherein said additive metallization is performed by electroplating.

125. The method of claim 113 further comprising fabricating interconnect wiring between said substrate and said signal wiring layer.

126. The method of claim 113 further comprising fabricating interconnect wiring between said signal wiring layer and chips mounted on said substrate.

127. A method of forming a chip carrier, said method comprising:

forming a first insulating layer on both sides of a substrate and in at least one through-hole of said substrate;

forming a conductive plane over said first insulating layer and in at least one through-hole of said substrate;

forming a second insulating layer over said conductive plane and in at least one through-hole of said substrate; and

forming a signal wiring layer over said second insulating layer and in at least one through-hole of said substrate.

128. The method of claim 127 further comprising forming a third insulating layer over said signal wiring layer and in at least one through-hole of said substrate.

129. A method of forming a chip carrier, said method comprising:

forming a first insulating layer on both sides of a substrate and in at least one through-hole of said substrate;

forming a first conductive plane over said first insulating layer and in at least one through-hole of said substrate;

forming a second insulating layer over said first conductive plane and in at least one through-hole of said substrate;

fabricating signal lines over said second insulating layer and in at least one through-hole of said substrate;

forming a third insulating layer over said signal lines and in at least one through-hole of said substrate;

forming a second conductive plane over said third insulating layer and in at least one through-hole of said substrate;

forming a fourth insulating layer over said second conductive plane and in at least one through-hole of said substrate; and

mounting a plurality of integrated circuit chips over said fourth insulating layer.

130. The method of claim 129 further comprising fabricating interconnect wiring between said signal lines and said integrated circuit chips.

131. The method of claim 129 further comprising fabricating interconnect wiring between said signal lines and active and/or passive components on said substrate.